IN THE SPECIFICATION:

Amend the paragraph beginning at page 4, line 21 and ending at page 5, line 21 as follows:

A semiconductor device according to this invention has peripheral electrodes (for example, peripheral electrode pads 1a and 1b ~~1~~ in the embodiment described later) formed on a periphery of a semiconductor chip; internal electrodes (internal electrode pads 5, for example) formed inside the peripheral electrodes on the semiconductor chip; and circuits (metal layer 4b, for example,) formed in the semiconductor chip. In this semiconductor device, the peripheral electrodes are connected to the circuits by an internal line (metal layer 4a, for example), and the internal electrodes are connected to the circuits and the peripheral electrodes by the internal line. The semiconductor device with this structure is compatible with both a packaging technology using wire bonding and a CSP technology using rewiring. Further, if the internal electrodes are connected to area array electrodes (land pads 3, for example) by rewired lines, the area array electrodes are connected to the circuits without via the peripheral electrodes, and therefore the line lengths can be short. This structure allows preventing short-circuit between two rewired lines or between the rewired

line and the area array electrodes. It also allows suppressing problems such as signal delay, line interference, and increased noise.

Amend the paragraph beginning at page 11, line 12 and ending at page 12, line 1 as follows:

As shown in Fig. 1, on the periphery of the semiconductor chip 10 are formed a plurality of peripheral electrode pads ~~1~~ 1a and 1b that are peripheral electrodes. The peripheral electrode pads ~~1~~ 1a and 1b are connected to various internal circuits (not shown) formed in the semiconductor chip 10 by internal lines (not shown). When inspecting the internal circuits of the semiconductor chip 10, the peripheral electrode pads 1a and 1b ~~1~~ are used also as input/output terminals for inputting and outputting inspection signals where probe terminals of an inspection device are brought into contact.

Amend the paragraph at page 12, lines 2-19 as follows:

On the inner side of the semiconductor chip 10 surrounded by the peripheral electrode pads 1a and 1b ~~1~~ are formed internal electrode pads 5. The internal electrode pads 5 are connected to the internal circuits and the peripheral electrode pads 1b ~~1~~ via

the internal lines. In Fig. 1, only internal lines 4 connecting the internal electrode pads 5 to the peripheral electrode pads 1b ~~1~~ are shown by broken lines. The internal electrode pads 5 are preferably as small as possible since a large principal surface increases electrical interference with the internal lines and reduces margins for the internal lines. The peripheral electrode pads 1a and 1b ~~1~~, on the other hand, need to have a size large enough to meet the accuracy limit of a wire bonding device. Accordingly, the principal surfaces of the internal electrode pads 5 are preferably smaller than those of the peripheral electrode pads 1a and 1b ~~1~~. Peripheral electrodes 1a are peripheral electrodes which are not connected to internal electrode pads 5, and peripheral electrodes 1b are peripheral electrodes which are connected to internal electrode pads 5 via internal lines.

Amend the paragraph beginning at page 12, line 20 and ending at page 13, line 7 as follows:

Fig. 2 is a fragmentary sectional view of the semiconductor chip 10 according to this embodiment before rewiring and land pad formation are performed. It is a cross-sectional view along line II-II in Fig. 1. In this embodiment, metal layers 4a and 4b are formed in different layers inside silicon 7. The metal layers 4a and 4b are connected by a via 4c. The metal layer 4a

and the via 4c are internal lines to connect the internal circuits formed inside the chip to each of the peripheral electrode pads 1b ~~1~~ and the internal electrode pads 5. The metal layer 4b is a line of the internal circuit formed inside the chip. The metal layers 4a and 4b are formed by aluminum (Al), for example.

Amend the paragraph at page 13, lines 8-18 as follows:

An insulating layer 6 is formed at the top surface of the silicon 7. A passivation layer (not shown) is generally formed directly under the insulating layer 6. The insulating layer 6 is formed by polyimide, for example. The insulation layer 6 has openings in the positions corresponding to the periphery of the semiconductor chip 10. The metal layer 4a is partly exposed in the openings of the insulating layer 6. The exposed portions of the metal layer 4a serve as the peripheral electrode pads 1b ~~1~~.

Amend the paragraph at page 13, lines 19-25 as follows:

Besides the openings for the peripheral electrode pads 1b ~~1~~, the insulating layer 6 has openings in the inner region of the semiconductor chip 10 to create the connection with land pads (not shown). The metal layer 4a is partly exposed in the

openings. The exposed portions of the metal layer 4a serve as the internal electrode pads 5.

Amend the paragraph beginning at page 13, line 26 and ending at page 14, line 11 as follows:

The semiconductor chip 10 in this state may be connected to external terminals via the peripheral electrode pads 1a and 1b ~~1~~ by wire bonding without rewiring and forming land pads. The semiconductor chip 10 may also be connected to external terminals via land pads after rewiring and land pad formation. Accordingly, the semiconductor chip 10 in this embodiment is processable by wafer level CSP packaging using rewiring technique, which has been difficult for a semiconductor with multiple pins, while maintaining compatibility with conventional packaging using wire bonding technique.

Amend the paragraph at page 14, lines 15-24 as follows:

Besides the peripheral electrode pads ~~1~~ 1a and 1b and the internal electrode pads 5, rewired lines 2 and land pads 3 which are area array electrodes are formed entirely in the semiconductor chip ~~1~~ 10. The rewired lines 2 are formed, for example, by depositing a copper or aluminum coating by

sputtering, and then etching the coating to form a given pattern. The land pads 3 are plated films formed by plating, for instance. In this embodiment, the land pads 3 comprise two types: land pads 3a and land pads 3b.

Amend the paragraph at page 15, lines 8-20 as follows:

The land pads 3b, on the other hand, are connected to the internal circuits not via the peripheral electrode pads 1b ~~1~~. The land pads 3b and the internal circuits are connected via the rewired lines 2, internal electrode pads 5, and the internal lines 4. Accordingly, the line lengths between the land pads 3b and the internal circuits are shorter than those between the land pads 3a and the internal circuits. It allows preventing short-circuit between two rewired lines or between the rewired line and the area array electrodes. It also allows suppressing problems such as signal delay, line interference, and increased noise.

Amend the paragraph beginning at page 17, line 14 and ending at page 18, line 1 as follows:

Now, a case where the semiconductor chip 10 is connected to external terminals via the peripheral electrode pads ~~1~~ by wire

bonding will be explained with reference to Fig. 7. In this case, CSP processing using rewiring technique as shown in Fig. 3 is not performed. The semiconductor chip 10 is mounted on a substrate 30 with the chip surface having the peripheral electrode pads 1 facing up. The peripheral electrode pads 1 are connected to terminals on the substrate 30 by bonding wires 32. After wire bonding, the semiconductor chip 10 is sealed by resin 33. The substrate 30 has solder balls 31 formed above lines in the bottom substrate surface.

Amend the paragraph at page 18, line 2-19 as follows:

When inspecting the semiconductor device, probe terminals of an inspection device are brought into contact with the electrodes of the semiconductor device to input and output signals. It is unfavorable to contact the prove terminals with the land pads 3 formed in the semiconductor chip 10. This is because contact pressure by the probe terminals can destroy the circuits below the land pads 3 during inspection. The semiconductor chip 10 in this embodiment can avoid the circuit destruction problem since the peripheral electrode pads 1 on the chip periphery can be used as terminals for inspection even when the connection with external terminals is made by the land pads 3. Although the circuit destruction problem does not occur if

no circuit is formed below the land pads 3, this decreases the efficiency of circuit design and thus fails to meet the demand for higher integration.

Amend the paragraph beginning at page 18, line 20 and ending at page 19, line 7 as follows:

This embodiment of the present invention employs a connection structure where some of the peripheral electrode pads ~~1~~ are connected to the land pads 3b via the internal electrode pads 5, which allows shorter line lengths. Terminals for inputting and outputting such signals that can be significantly affected by voltage drop preferably have short line lengths. Thus, it is preferred that such terminals are preferentially allocated to the land pads 3b connected to the internal circuits via the internal electrode pads 5. The terminals for inputting and outputting signals significantly affected by voltage drop include power supply terminals, ground terminals, and clock terminals.

Amend the paragraph at page 19, lines 8-17 as follows:

On the other hand, the land pads 3b connected to the internal circuits via the internal electrode pads 5 as shown in

Fig. 3 are not suitable for use as input/output terminals for high-frequency signals such as RF signals. This is because the internal lines 4 connecting the internal circuits and the peripheral electrode pads ~~1~~ 1b become redundant lines when the land pads 3b are connected to external terminals, thereby generating incorrect impedance to distort signal waveforms.

Amend the paragraph beginning at page 19, line 25 and ending at page 20, line 12 as follows:

An example of a manufacturing process for the semiconductor chip 10 will be briefly explained hereinbelow. First, the internal lines 4 are formed in the semiconductor wafer 100. Next, the passivation layer and the insulating layer 6 having openings where the peripheral electrode pads ~~1~~ will be exposed and where the land pads will be formed are formed at a surface of the semiconductor wafer 100. The insulating layer 6 is formed by photoresist coating, prebaking, exposure and development by photolithography process, and postbaking. After that, a copper coating is deposited by sputtering above the insulating layer 6 and the peripheral electrode pads ~~1~~.

Amend the paragraph beginning at page 20, line 25 and ending at page 21, line 5 as follows:

Though the land pads 3 which are area array electrodes are uniformly arranged all over the semiconductor chip 10 ~~1~~ in the above embodiment, it is not restricted thereto, and nonuniform arrangement of the land pads 3 is also possible. For example, the center portion of the semiconductor chip 10 ~~1~~ may have no land pads 3.